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# High-Efficiency Wilkinson-Power-Combining Class-EF Amplifier with Lumped-Element Load Network

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**Abstract**—This paper presents a design strategy to incorporate the load network of Class-EF power amplifier (PA) into a complex-impedance-terminated Wilkinson power combiner (WPC) in order to reduce the circuit complexity and footprint. To further reduce the circuit footprint, the WPC and the Class-EF PA's load network are designed using lumped elements as opposed to transmission lines typically employed in the classical designs. The proposed circuit provides an impedance matching from 50  $\Omega$  to a complex impedance at the fundamental frequency and a short-circuit termination at the second harmonic. The new topology exhibits a band-pass frequency response instead of low/high-pass as in the conventional WPCs, thus enabling suppression of unwanted signals at low and high frequencies. Closed-form design equations, derived using even/odd mode analysis, are given along with a design example. Driven by a 3-GHz continuous-wave input signal, the proposed PA delivers 41.5-dBm output power with DC-to-RF efficiency of 83.6% at 3.9-dB compressed gain of 15.2 dB.

**Keywords**—Class EF; GaN; high efficiency; lumped element; power amplifier; power combiner; Wilkinson.

## I. INTRODUCTION

With power amplifier (PA) consuming the majority of the power in a wireless transceiver chain, it is important to ensure that the PA operates with utmost efficiency. Switch-mode PAs such as Class E [1] and harmonically tuned PAs such as Class F [2] have been extensively used for high-efficiency transmitters. These PAs can theoretically achieve 100% DC-to-RF efficiency since the switch voltage and current waveforms do not overlap, thus leading to zero power dissipation within the switch. The Class-EF PA, reported in [3]-[4], inherits the advantages offered by the Class E and Class F, namely (i) low peak switch voltage, hence allowing the PA to be operated at high output power, (ii) high load resistance, hence minimizing the loss introduced by the matching network, and (iii) soft switching, hence minimizing the power dissipation during OFF-to-ON transition.

To boost the output power of the PA, power-combining structures such as the isolated Wilkinson power combiner (WPC) [5] and non-isolated quarter-wave transmission lines (QWTLs) power combiner [6] can be utilized. The WPC circuit gains popularity due to its simple topology that is comprised of two identical QWTLs and an isolation resistor, and its superb intrinsic characteristics, namely high isolation and excellent impedance matching at both input and output ports. However, it is impractical to implement it at low RF/microwave frequencies

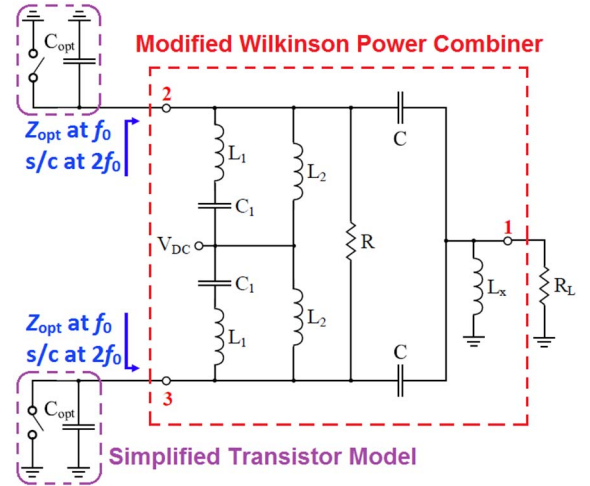


Fig. 1. The proposed lumped-element power-combining Class-EF amplifier.

due to the large footprint of the QWTLs, particularly when realized in integrated circuit (IC) format where chip area is at a premium. The typical solution to this problem is by replacing each QWTL with its  $\pi$  equivalent lumped model, i.e., either C-L-C network with low-pass frequency response or L-C-L network with high-pass frequency response, [7]-[8].

In this paper, we propose a compact architecture that allows the load network of the Class-EF PA to be fully incorporated into the WPC structure (Fig. 1). A new exact analysis is developed to allow the load resistance  $R_L$  (typically 50  $\Omega$ ) connected at port 1 to be transformed to a complex impedance  $Z_{opt}$  (as opposed to purely resistive impedance assumed in [7]) at the fundamental frequency ( $f_0$ ) while presenting a short-circuit termination to ports 2 and 3 at  $2f_0$  as required by the Class-EF mode. The proposed circuit makes use of the L-C-L (instead of the more widely adopted C-L-C) network since it can double as a DC-feed inductance ( $L_2$  in Fig. 1) to bias the drain of the transistors, and as a DC-blocking capacitance ( $C$  in Fig. 1) to prevent the DC signal from leaking out to the output. Compared with the classical arrangement wherein two identical Class-EF PAs are connected directly to the WPC, the proposed circuit requires fewer components, hence leading to a compact circuit, lower implementation cost, and improved performance due to reduced component parasitics. Additionally, the design methodology presented in this paper requires no tuning of the component values, which significantly shortens the design time.

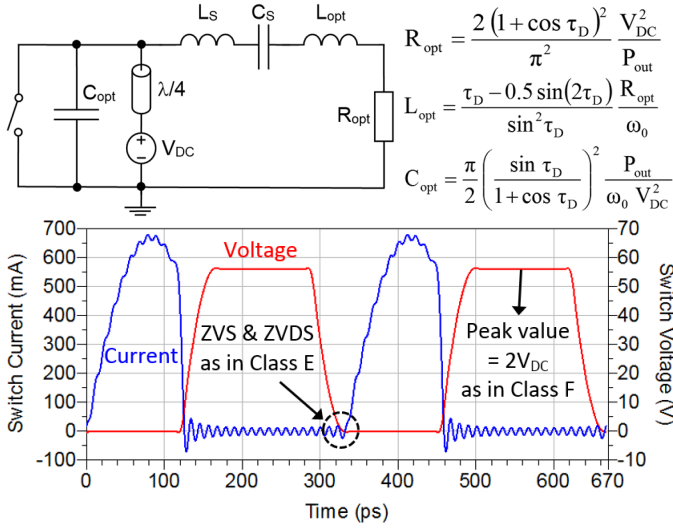


Fig. 2. Idealized Class-EF power amplifier: basic circuit (top), switch current and voltage waveforms for given specifications:  $\tau_D = 48.5^\circ$ ,  $f_0 = 3$  GHz,  $P_{out} = 5$  W, and  $V_{DC} = 28$  V (bottom).

## II. BASIC CONCEPTS

### A. Class-EF Power Amplifier

The circuit topology of the Class-EF PA and its idealized switch current and voltage waveforms are shown in Fig. 2. Here, a switch and a shunt capacitor  $C_{opt}$  are used to model a transistor with  $C_{opt}$  representing the transistor's output capacitance. The QWTL in Fig. 2 has a pivotal role to supply a DC signal as well as to present a short-circuit and open-circuit terminations to even-harmonic and odd-harmonic components, respectively. The series resonator  $L_s C_s$  is tuned at  $f_0$ , thus facilitating a short circuit at  $f_0$  and a high impedance at harmonic frequencies. As a result, a complex impedance  $Z_{opt} = R_{opt} + j\omega_0 L_{opt}$ , a short circuit, and a high impedance are presented to the drain of the transistor at  $f_0$ ,  $2nf_0$ , and  $(2n+1)f_0$ , respectively. A set of equations to determine the values of  $R_{opt}$ ,  $L_{opt}$ , and  $C_{opt}$  is given in Fig. 2, where  $P_{out}$  is the output power,  $V_{DC}$  is the DC supply voltage, and  $\tau_D$  is a dead time, [3]. From Fig. 2, it can be observed that the peak switch voltage is  $2 \times V_{DC}$  that is lower than the Class E's, i.e.  $3.562 \times V_{DC}$ , and that the zero voltage switching (ZVS) and zero voltage derivative switching (ZVDS) conditions are fulfilled.

Despite the advantages offered by the Class EF, the total series inductance  $L_{opt} + L_s$  (Fig. 2) is typically of large value. This large inductance is accompanied with a large equivalent series resistance (ESR) whose value is often comparable to the optimum load resistance ( $R_{opt}$ ), thus leading to significant power losses that will degrade the overall PA efficiency.

### B. Wilkinson Power Combiner with Complex Impedance Termination

The lumped-element WPC shown in Fig. 3 is formed by replacing each QWTL in the classical WPC arrangement with an L-C-L  $\pi$  network. The circuit components values are derived using even/odd mode analysis, wherein  $R_L$  that is connected at

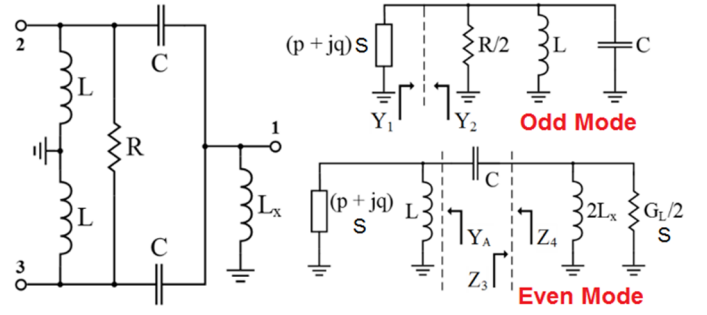


Fig. 3. WPC with complex impedance termination: basic circuit (left), equivalent circuits for even/odd mode excitations (right).

port 1 is transformed to the Class-EF's optimum impedance  $Z_{opt} = R_{opt} + j\omega_0 L_{opt} = (a + jb) \Omega$  seen by ports 2 and 3. Compared with [7] wherein  $R_L$  is transformed to a purely resistive impedance, this strategy removes the need for additional matching circuits, thus resulting in a compact circuit. For the analysis to provide a complex conjugate match, ports 2 and 3 are terminated with an admittance  $(p + jq) S$  where

$$p + jq = \frac{1}{a - jb} = \frac{a + jb}{a^2 + b^2} \quad (1)$$

For odd mode, the plane of symmetry acts as a virtual short circuit, Fig. 3. Components  $L_x$  and  $G_L (= 1/R_L)$  at port 1 are short-circuited and therefore can be removed from the circuit. The resistor  $R$  is split into two, yielding  $R/2$ . Equating the real components of  $Y_1$  and  $Y_2$  yields (2), and equating the imaginary component of  $Y_1$  to the complex conjugate of  $Y_2$  results in (3).

$$R = 2/p \quad (2)$$

$$L = \frac{1}{\omega_0 (q + \omega_0 C)} \quad (3)$$

For even mode, the plane of symmetry acts as a virtual open circuit, hence  $R$  can be neglected, Fig. 3. Using (3), the admittance  $Y_A$  can be simplified to (4), and the impedances  $Z_3$  and  $Z_4$  are then determined as in (5)-(6).

$$Y_A = p + j \left( q - \frac{1}{\omega_0 L} \right) = p - j\omega_0 C \quad (4)$$

$$Z_3 = \frac{2\omega_0 L_x (\omega_0 L_x G_L + j)}{1 + (\omega_0 L_x G_L)^2} \quad (5)$$

$$Z_4 = \frac{-j}{\omega_0 C} + \frac{1}{Y_A} = \frac{-j}{\omega_0 C} + \frac{p + j\omega_0 C}{p^2 + (\omega_0 C)^2} \quad (6)$$

Finally,  $L_x$  and  $C$  can be obtained from (5)-(6).

$$L_x = R_L C/p \quad (7)$$

$$C = \frac{1}{\omega_0} \sqrt{\frac{p}{2 R_L}} \quad (8)$$

From (2), (3), (7), and (8), it can be seen that  $L$  is dependent on both the conductance  $p$  and the susceptance  $q$  while  $R$ ,  $L_x$ , and  $C$  are dependent on  $p$  only.

### C. Power-Combining Class-EF Amplifier

In the classical arrangement, two identical Class-EF PAs in Fig. 2 are directly connected to ports 2 and 3 of the WPC in Fig.

3 with the PA and WPC designed and optimized individually. In contrast to this, the proposed PA configuration in Fig. 1 is formed by merging the circuits in Figs. 2 and 3, wherein the load network of the Class-EF is incorporated into the WPC circuit while preserving the Class-EF's high efficiency and the WPC's high isolation characteristics. A grounded series resonator  $L_1C_1$  is tuned at  $2f_0$  (9) to facilitate a short-circuit termination at ports 2 and 3. At  $f_0$ , this resonator provides a net capacitance  $C_{eq}$  given in (10). This capacitance is tuned out by a shunt inductor  $L_t$  at  $f_0$  (11). The inductance  $L$  of the WPC in Fig. 3 and  $L_t$  are then combined into  $L_2$  defined in (12). The value of  $L_t$  can be chosen arbitrarily, thus providing a degree of design freedom. Subsequently, the values of  $L_1$ ,  $C_1$ , and  $L_2$  can be determined. The series capacitor  $C$  doubles as a DC-blocking capacitance and the shunt inductor  $L_2$  doubles as a DC-feed inductance, hence dispensing the need for a QWTL as in Fig. 2.

$$L_1 = \frac{1}{4 \omega_0^2 C_1} \quad (9)$$

$$C_1 = 0.75 C_{eq} \quad (10)$$

$$C_{eq} = \frac{1}{\omega_0^2 L_t} \quad (11)$$

$$L_2 = \frac{L L_t}{L + L_t} \quad (12)$$

### III. DESIGN EXAMPLE AND VERIFICATION

To verify the concept and the accuracy of the analysis described in Section II, the PA circuit in Fig. 1 was simulated in Advanced Design System (ADS) with the switch and the shunt capacitor  $C_{opt}$  replaced by Cree's CGH40010F GaN transistor model. To obtain maximum power added efficiency (PAE), a load pull simulation was performed on the device. The chief objective here is to find an optimum fundamental-frequency load impedance ( $Z_{opt}$ ) while setting the second-harmonic load impedance to zero. For  $V_{GG} = -2.6$  V and  $V_{DC} = 28$  V, the value of  $Z_{opt}$  extracted at the drain node of the transistor was found to be  $(10.7 + j21.4) \Omega$  at 3 GHz. This gives 83.2% drain efficiency (DE), 81.2% PAE, and 38.5-dBm output power.

The simulated S-parameters of the modified WPC circuit depicted in the boxed section of Fig. 1 are shown in Fig. 4 with its component values given in Table I. The values of  $R$ ,  $L$ ,  $L_x$ , and  $C$  of Fig. 3 are first calculated using (2), (3), (7), and (8). For a prescribed  $L_t$ , the values of  $L_1$ ,  $C_1$ , and  $L_2$  of Fig. 1 are then calculated using (9), (10), and (12). From the inspection of Fig. 4, return losses at both input and output ports are excellent and the isolation between the two input ports is high. With a transmission zero produced at 6 GHz ( $2f_0$ ) due to the added series resonators  $L_1C_1$ , the high-pass frequency response of the original L-C-L network turns into a band pass, thus enabling suppression of unwanted signals at low and high frequencies.

Fig. 5 shows the complete circuit schematic of the proposed PA including the input matching network that is comprised of  $C_m$  and  $L_m$  with  $C_m$  doubling as a DC-blocking capacitance. A resistor  $R_{GG} = 300 \Omega$  is used to bias the gate of each transistor and help improve the PA stability. The PA performance in terms of output power, gain, DE, and PAE is shown in Fig. 6 with the

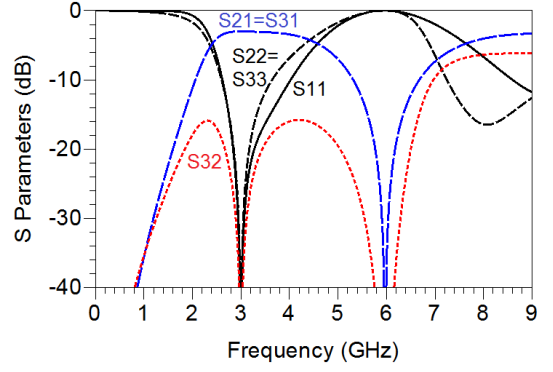


Fig. 4. Simulated S-parameters of the complex-impedance-terminated WPC for  $Z_{opt} = (10.7 + j21.4) \Omega$ .

TABLE I. CIRCUIT COMPONENT VALUES

Fig. 3	Fig. 1	Fig. 5
$R = 107 \Omega$	$R = 107 \Omega$	$R = 107 \Omega$
$C = 0.725$ pF	$C = 0.725$ pF	$C = 0.725$ pF
$L_x = 1.94$ nH	$L_x = 1.94$ nH	$L_x = 1.94$ nH
$L = 1.04$ nH	$L_1 = 1.67$ nH	$L_1 = 1.67$ nH
	$C_1 = 0.42$ pF	$C_1 = 0.42$ pF
	$L_2 = 0.86$ nH	$L_2 = 0.86$ nH
		$C_m = 2.65$ pF
		$L_m = 0.49$ nH

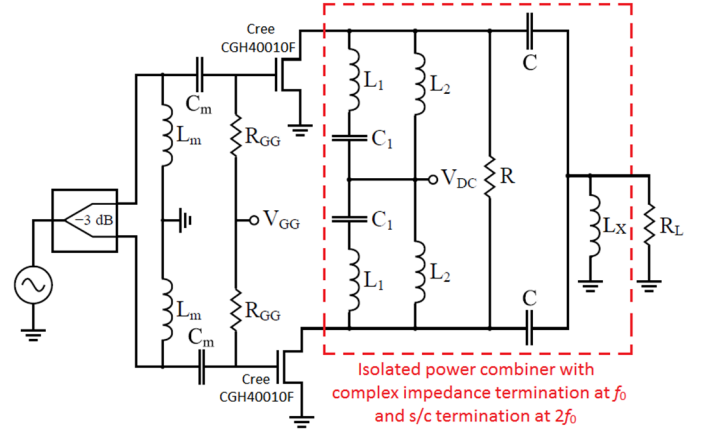


Fig. 5. Complete circuit schematic.

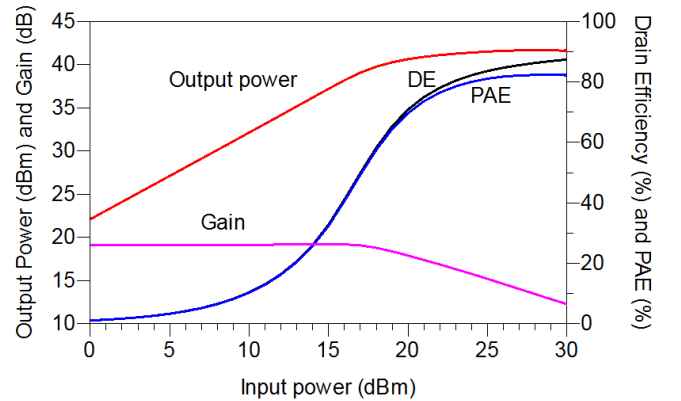


Fig. 6. Simulated output power, gain, DE, and PAE versus input power ( $V_{GG} = -2.6$  V,  $V_{DC} = 28$  V,  $f_0 = 3$  GHz).

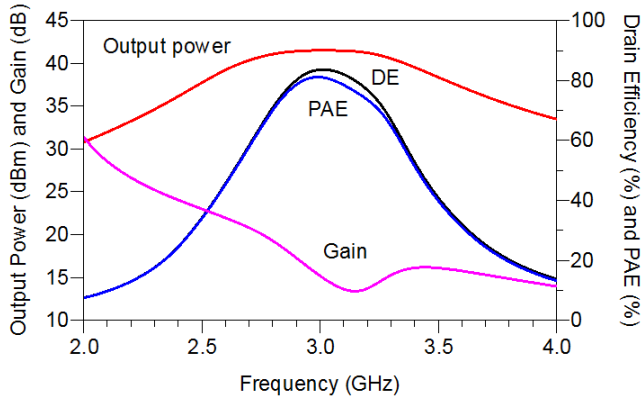


Fig. 7. Simulated output power, gain, DE, and PAE versus frequency ( $V_{GG} = -2.6$  V,  $V_{DC} = 28$  V, input power = 25 dBm).

input power swept from 0 to 30 dBm. The PA exhibits 83.6% DE, 81.1% PAE, and 41.5 dBm output power at 3.9-dB compressed gain of 15.2 dB. These results agree well with the load-pull simulation where the output power of the individual PA is 3 dB lower (38.5 dBm vs. 41.5 dBm) at a similar PAE level. The frequency response of the PA is shown in Fig. 7 with PAE higher than 70% and relatively constant output power achieved across a 450 MHz frequency range from 2.8 GHz to 3.25 GHz.

#### IV. CONCLUSION

The analysis of a novel Wilkinson-power-combining Class-EF amplifier with a compact lumped-element load network has been presented along with a holistic design procedure. The proposed PA circuit provides an impedance matching from  $50 \Omega$  to a complex impedance at the fundamental frequency and a short-circuit termination at the second harmonic frequency. The

PA's optimum fundamental-frequency load impedance is obtained from a load pull to maximize efficiency and output power. Closed-form design equations, derived using even/odd mode analysis, have been presented along with a practical design example using commercially available GaN transistors.

#### ACKNOWLEDGMENT

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